

Amendments to the Claims

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claims 1-5 (Canceled)

Claim 6 (Currently Amended): A semiconductor device comprising:

first and second gates formed on active regions of a substrate, said first and second gates each consisting of a refractory metal layer on a polysilicon layer;

a field oxide formed on the substrate between said first and second gates;

side walls formed on side surfaces of said first and second gates, said side walls being a silicon oxide film;

a protective layer formed selectively on said field oxide to prevent overetching of said field oxide,

said protective layer being a conductive layer and having an edge thereof on said field oxide, whereby edges of said protective layer are not covered by ~~side walls~~ sidewall spacers; and

an insulating layer, a contact hole, and a connecting wire formed above a surface of the substrate.

Claim 7 (Previously Presented): The semiconductor device of claim 6, wherein said protective layer is a polysilicon layer.

Claim 8 (Previously Presented): The semiconductor device of claim 6, wherein said protective layer is formed on said field oxide only.

Claim 9 (Previously Presented): The semiconductor device of claim 6, wherein said first and second gates are MOSFET gates.

Claim 10 (Canceled)

Claim 11 (Currently Amended): A semiconductor device comprising:

- a gate formed on an active region of a substrate;
- a field oxide formed on the substrate adjacent the active region;
- a protective layer formed on said field oxide to prevent overetching of said field oxide,
- said protective layer being a conductive layer and having an edge thereof on said field oxide, whereby edges of said protective layer are not covered by ~~side-walls~~ sidewall spacers; and
- an insulating layer, a contact hole, and a connecting wire formed above a surface of the substrate,

said protective layer being formed on said field oxide only.

Claim 12 (Previously Presented): The semiconductor device of claim 11, wherein said protective layer is a polysilicon layer.

Claim 13 (Previously Presented): The semiconductor device of claim 11, wherein said gate is a MOSFET gate.

Claim 14 (Currently Amended): The semiconductor device of claim 11, further comprising ~~side walls~~ sidewall spacers formed on side surfaces of said gate, said ~~side walls~~ sidewall spacers being covered by said insulating layer.

Claim 15 (Previously Presented): The semiconductor device of claim 11, further comprising an additional gate formed on the substrate, said field oxide being formed on the substrate between said gate and said additional gate.

Claim 16 (Currently Amended): A semiconductor device comprising:

a gate formed on an active region of a substrate, said gate consisting of a refractory metal layer on a polysilicon layer;

sidewall spacers ~~side walls~~ formed on side surfaces of said gate, said sidewall spacers ~~side walls~~ being a silicon oxide film;

a field oxide formed on the substrate adjacent the active region;
a protective layer formed on said field oxide to prevent overetching of said field oxide,
said protective layer being a conductive layer and having an edge thereof on said field oxide, whereby edges of said protective layer are not covered by sidewall spacers ~~side walls~~; and
an insulating layer, a contact hole, and a connecting wire formed above a surface of the substrate,
said protective layer being formed on said field oxide only.

Claim 17 (Previously Presented): The semiconductor device of claim 16, wherein said protective layer is a polysilicon layer.

Claim 18 (Previously Presented): The semiconductor device of claim 16, wherein said gate is a MOSFET gate.

Claim 19 (Previously Presented): The semiconductor device of claim 16, further comprising an additional gate formed on the substrate, said field oxide being formed on the substrate between said gate and said additional gate.